VALUE CONSTRAINT AND MONOTONE CIRCUIT

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1. Overview

This paper talks about that monotone circuit is P-Complete. Decision problem that include P-Complete is mapping that classify input with a similar property. Therefore equivalence relation of input value is important for computation. But monotone circuit cannot compute the equivalence relation of the value because monotone circuit can compute only monotone function. Therefore, I make the value constraint explicitly in the input and monotone circuit can compute equivalence relation. As a result, we can compute P-Complete problem with monotone circuit. We can reduce implicit value constraint to explicit with logarithm space. Therefore, monotone circuit is P-Complete.

2. Monotone circuit and Equivalence relation

First, I show that a monotone circuit cannot compute equivalence relation. Decision problem that include P-Complete is mapping of $\{0,1\}^* \to \{0,1\}$ and classify $\{0,1\}^*$ to two sets. It is important to classify $\{0,1\}$ as the element of $\{0,1\}^*$. But monotone circuit cannot classify $\{0,1\}$.

Theorem 1. *Monotone circuit cannot classify equivalence relation.*

Proof. I prove it using reduction to absurdity. We assume that monotone circuit can classify equivalence relation. From assumptions, this monotone circuit output same value when input value is $(0,0),(1,1)$.

But monotonicity of monotone circuit $0 \wedge 0 = 0 \vee 0 = 0, 1 \wedge 1 = 1 \vee 1 = 1$ makes different output with inputs $(0,0),(1,1)$, and contradicts a condition to classify equivalence relation.

Therefore, this theorem was shown than reduction to absurdity. $\square$

The reason why a monotone circuit has such a limit is that monotone circuit do not have a Not gate. Monotone circuit cannot compute value exclusivity, therefore monotone circuit cannot classify equivalence relation.

3. Flatten problem

Next, I show that how to compute equivalence relation with monotone circuit. To reduce implicit value constraint explicitly, we can compute equivalence relation with monotone circuit.

Definition 2. I will use the term "Flatten input" as changing each value of an input (Target input) of problem (Target problem) to
$$\begin{cases} 0 \to 10 \\ 1 \to 01 \end{cases}$$

And I will use the term "Flatten problem" as that problem that reduce object input to flatten input.

That is, Flatten input is the input that expressed a value of the target input with some values. Therefore, implicit constraint of target input value become explicit flatten input values relations.

To reduce flatten input from target input, monotone circuit can classify equivalence relation.

Theorem 3. *Monotone circuit can classify flatten input value.*

Proof. I make a monotone circuit classifying flattening input. Target input is (x, y) and flatten input is $(x_0, x_1, y_0, y_1) = (\overline{x}, x, \overline{y}, y)$, then monotone circuit classifying flattening input is $((x_0 \wedge y_0) \vee (x_1 \wedge y_1))$. $\square$

4. Reduce DTM to Boole circuit with Tableau

I omit the proof that reduce DTM to Boole circuit with Tableau. Refer to theorem 9.30 of references[1] for the details. Boole circuit that reduce DTM Tableau only use Not gate at the input values flattening.

5. Flattening DTM and Monotone circuit

Compute DTM with monotone circuit.

Theorem 4. *To flat target input, monotone circuit can compute this problem.*

Proof. It is clear from Boolean circuit structure that reduce DTM, I omit the proof that reduce DTM to Boole circuit with Tableau. The Boolean circuit that reduce DTM only use not gate at input values flattening. Therefore, not gate is not necessary to compute flatten input. $\square$

We can reduce target problem to flatten problem by using LDTM.

Theorem 5. *Target problem can reduce to flatten problem by using LDTM. Therefore, Flatten problem that reduce P-Complete problem is P-Complete.*

Proof. I make that LDTM to reduce target input to flatten input. When this LDTM receives target input, LDTM change each target input value to $0 \rightarrow 10, 1 \rightarrow 01$ and output these values. LDTM must record input value position and status. These data use logarithm space and LDTM can record these data. Therefore, LDTM can compute these reduction, and flatten problem that reduce P-Complete problem is P-Complete. $\square$

Size of Monotone circuit that compute flatten problem is at most polynomial size of Boolean circuit that compute target problem.

Theorem 6. *Monotone circuit that is polynomial size can compute flatten problem that reduce P-Complete problem.*

Proof. Mentioned above 4, monotone circuit that compute flatten problem is the circuit that delete not gate from Boolean circuit that reduce DTM tableau which compute target problem. Size of Boolean circuit that compute target problem is polynomial size. Therefore, size of monotone circuit that compute flatten problem is polynomial size. $\square$

Theorem 7. *Monotone circuit is P-Complete.*

Proof. Monotone circuit is in P clearly.

Mentioned above 56, To flattening P-Complete problem, we can reduce these problem to monotone circuit with polynomial size. Therefore, monotone circuit is P-Complete. □

References

[1] Michael Sipser, (translation) OHTA Kazuo, TANAKA Keisuke, ABE Masayuki, UEDA Hiroki, FUJIOKA Atsushi, WATANABE Osamu, Introduction to the Theory of COMPUTATION Second Edition, 2008

[2] HAGIYA Masami, NISHIZAKI Shinya, Mechanism of Logic and Calculation, 2007